REMARKS/ARGUMENTS

Claim 3 has been canceled without prejudice.

Claims 4-10 are pending in the application.

Claim 4 has been rejected under 35 U.S.C. §102(b) as anticipated by Hshieh, U.S. Patent No. 5,907,776.

In response to the Office Action dated July 3, 2003, it was submitted that claim 4 is not anticipated by Hshieh because Hshieh does not show "selecting an active region in a major surface of a semiconductor body of a first conductivity type;" and "implanting dopants of a second conductivity type in all of said active region."

Responsive to the arguments set forth above, Figures 7I and 7J were cited by the Examiner as showing the distinguishing features of claim 4.

Claim 4 calls for the following combination of elements.

> A method for producing a vertical MOSFET, the method comprising:
>
> selecting an active region in a major surface of a semiconductor body of a first conductivity type;
>
> implanting dopants of a second conductivity type in all of said active region;
>
> forming a plurality of spaced channel region of said second conductivity type in said active region; and
>
> forming at least one source region of said second conductivity type in each of said channel regions.

When a vertical conduction MOSFET is in a blocking mode, the inherent P/N body diode (the junction of the channel regions and the epitaxial layer in which the channel regions are formed) depletes toward the source. If there is insufficient charge in the channel regions, punch-through occurs before avalanche breakdown is reached.

In a low voltage VDMOS device (Vertical Conduction Double Diffused MOS), this premature punch-through is normally prevented by using a higher channel dose and/or a deeper channel drive than might be otherwise required for a given avalanche breakdown value.

However, the higher channel dose results in a correspondingly higher threshold voltage V_{TH}; while a deeper channel drive increases channel length and thus channel resistance. The deeper channel drive also increases the depth of the JFET region between adjacent channel regions, thus reducing the optimum utilization of the epitaxial silicon.

The present invention is directed at a process for manufacturing a MOSFET in which punch-through is prevented without increasing channel dose or channel depth.

According to the invention, a depletion implant is formed in the top surface of the epitaxial silicon for a low voltage MOSFET prior to the formation of the channel and source diffusions. For example, a boron blanket implant will be used in an N channel VDMOS to reduce the net N type concentration, and an Arsenic or Phosphorous blanket implant is used in a P channel VDMOS. The depletion implant enables the use of a lower channel implant dose and/or a shorter channel drive without getting into a punch-through condition before avalanche voltage is reached. This technique will also lower channel resistance which, for low voltage MOSFETs (for example, 40 volts or less) is a significant portion of the device total on-resistance.

According to an aspect of the present invention, the depletion implant is applied at any time prior to the channel diffusion.

The novel depletion implant of the invention will put a uniform charge into the channel region, therefore preventing punch-through as described above.

The cited portion of Hshieh does not show a blanket implant or as called for by claim 4 an implant "in all of said active region." Rather Hshieh shows the implant step for forming the source regions of the device. Thus, Figs. 7I and 7J only show implants in some not all of said active region. This is clear from the fact that mask 86 covers portions of the active region that are not to receive dopants during the implantation. Reconsideration of claim 4 is requested.

Each of the remaining claims depends from claim 4 and, therefore, includes its limitations. Each of these claims includes additional limitations which in combination with those of claim 4 have not been shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 2, 2003:

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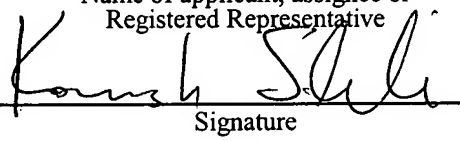
Name of applicant, assignee or Registered Representative



Signature

December 2, 2003

Date of Signature

SHW:KS:ck

Respectfully submitted,

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